

SEMICONDUCTOR DEVICE, AND DESIGN METHOD,
INSPECTION METHOD, AND DESIGN PROGRAM THEREFOR

BACKGROUND OF THE INVENTION

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Field of the Invention

The present invention relates to a semiconductor device and relates to a design method, an inspection method, and a design program therefor.

10 Description of the Related Art

Fig. 6 is a diagram showing an example of the layout for a semiconductor device, which is designed using a known automatic wiring tool. Fig. 7A is a diagram showing the wiring structure of area A1 in Fig. 6, and Fig. 7B is a sectional view along line J-J in Fig. 7A. Fig. 8A is a diagram showing the wiring structure of area A2 in Fig. 15 6, and Fig. 8B is a sectional view along line K-K in Fig. 8A.

In Fig. 6, reference numerals 100A to 100D indicate circuit blocks formed on a semiconductor substrate, and reference numerals 111 to 117 indicate wiring lines for connecting the circuit blocks 100A to 100D with each other. In the area A1 indicated by dashed lines, the wiring lines 111 to 113 extending in the horizontal direction on Fig. 20 6 intersect with the wiring lines 114 and 115 extending in the vertical direction on Fig. 6. In the area A2, the above wiring lines 114 and 115 intersect with the wiring line 117 extending in the horizontal direction on the figure, and this wiring line 117 is electrically connected to the wiring line 116 extending in the vertical direction on the figure.

As shown in Fig. 7A, the wiring lines 114 and 115 respectively have measurement electrodes 114b and 115b via extension wiring lines 114a and 115a, in a

manner such that the areas of the measurement electrodes 114b and 115b do not overlap those of the wiring lines 111 to 113 in plan view.

In addition, in the wiring structure shown in Figs. 8A and 8B, the wiring lines 114 and 115 are formed in the uppermost layer of the semiconductor device, the wiring 5 line 117 is formed between the third interlayer insulating film 103 and the second interlayer insulating film 102, and the wiring line 116 is formed between the second interlayer insulating film 102 and the first interlayer insulating film 101.

The wiring lines 116 and 117 are electrically connected to each other via a contact hole 105, which is formed through the second interlayer insulating film 102, at a 10 position where the wiring lines 116 and 117 intersect with each other in plan view. In the uppermost layer above this intersection of the wiring lines 116 and 117, a measurement electrode 118 is formed, which is electrically connected to the wiring line 117 via a contact hole 106 formed through the third interlayer insulating film 103.

In conventional voltage or logic measurements for the inside of semiconductor 15 devices, a thin metal needle is made to directly contact each wiring line on the surface of the semiconductor device, or secondary electrons obtained by irradiating the wiring line with an electron beam are measured. Typically, as shown in Fig. 7A, dedicated electrodes 114b and 115b for performing such a measurement are provided, and the measurement is performed via the electrodes 114b and 115b. However, in this case, 20 each electrode is generally provided at a position which the designer believes necessary; thus, the results obtained by the automatic wiring layout tool should be manually corrected, thereby increasing labor (or man-hour). In addition, as shown in Figs. 7A and 7B, space for forming the electrodes 114b and 115b and areas for providing the wiring lines 114a and 115a (for providing these electrodes) are also necessary.

25 However, in the above conventional methods of making a needle contact the

wiring line or irradiating the wiring line with an electron beam, the wiring lines other than those provided in the uppermost layer cannot be measured. In order to perform the measurement for the wiring lines formed in the second or lower layers, a hole for measurement (here, the contact hole 106) is formed through the third interlayer 5 insulating film 103 (see Figs. 8A and 8B), so as to connect the electrode 118 to the wiring line 116, and the measurement is performed by making a probe 108 contact the electrode 118. However, in the semiconductor devices using the recent multilayer wiring technique, wiring lines are crowded and wiring density in the uppermost layer is very high; thus, it is very difficult to secure an area for providing such a measurement 10 hole in the uppermost layer of the semiconductor device. Additionally, such an area for proving a measurement hole is manually searched for, thereby requiring a considerable amount of time.

In addition, Japanese Unexamined Patent Application, First Publication No. Sho 64-027241 discloses that a measurement terminal is provided in each unit cell of an 15 electric circuit; however, in recent circuit design, the unit cell is generally covered with a wiring layer for a power supply or the like, and it is difficult to secure an area for providing the measurement terminal.

Japanese Unexamined Patent Application, First Publication No. Hei 9-139471 discloses using an automatic layout tool for measurement terminals; however, in the 20 disclosed method, after completion of the wiring layout process, the layout operation is again performed by using a tool for searching for an area which satisfies specific conditions (i.e., an area where an electrode can be provided on the surface layer). In this case, if measurement terminals cannot be suitably arranged in the layout, correction of the entire design, such as reconsideration of the entire layout, is necessary. 25 Therefore, increase in labor according to the increase in the load of simulation is

inevitable, and thus it is difficult to put this method to practical use.

Japanese Unexamined Patent Application, First Publication No. Sho 62-076736 discloses preparing cells in which a measurement terminal is mounted on a small-scale logic circuit, and performing connection between all cells after suitably arranging the 5 cells in which no measurement terminal is mounted and the cells in which measurement terminals are mounted. However, in this case, each measurement terminal makes a pair with a logic circuit; thus, in the automatic wiring process, wiring cannot be produced in a layer above each circuit in the layout. In addition, the measurement terminal is not always mounted on each logic circuit (i.e., , and each logic circuit in which the 10 measurement terminal should be mounted is defined and selected; thus, it is difficult to automate the layout process.

SUMMARY OF THE INVENTION

In consideration of the above circumstances, an object of the present invention 15 is to provide a semiconductor device design method and design program for automatically determining layout of a semiconductor device which has measurement terminals for measuring voltage, logic state, or the like, on wiring lines for connecting the circuit blocks.

Another object of the present invention is to provide a semiconductor device 20 inspection method using measurement terminals which are arranged by the above semiconductor device design method.

Another object of the present invention is to provide a semiconductor device which is designed by the above semiconductor device design method.

Therefore, the present invention provides a design method of designing a 25 multilayer semiconductor device which includes a plurality of circuit blocks formed on a

semiconductor substrate, the method comprising the steps of:

registering measurement terminals as cells in design rules, together with the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and the measurement terminal is
5 connectable to a wiring line for connecting any two of the circuit blocks, which is formed in any layer of the semiconductor device;

planar-arranging the measurement terminals and the circuit blocks; and establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.

10 Typically, in the step of establishing the connection of each wiring line, the connection is performed based on a net list which stores data of each measurement terminal and terminations of a wiring line on which the measurement terminal is provided.

The present invention also provides an inspection method of inspecting a
15 multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the method comprising the step of:

performing inspection via an electrode of a measurement terminal, wherein the measurement terminal is provided on a wiring line which extends from one of the circuit blocks, the electrode is formed in an uppermost layer of the semiconductor device, and
20 the measurement terminal has a pad in each of the remaining layers of the semiconductor device, and the pads are electrically connected with each other via contact holes, each contact hole passing through each insulating film of the semiconductor device.

In a preferable example, the step of performing inspection includes measuring at least one of voltage and logic state of the wiring line on which the measurement terminal is provided, by one of making a probe contact the electrode of the measurement

terminal and irradiating the electrode with an electron beam.

The present invention also provides a design program for making a computer execute an operation of designing a multilayer semiconductor device which includes a plurality of circuit blocks formed on a semiconductor substrate, the operation comprising
5 the steps of:

registering measurement terminals as cells in design rules, together with the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device, and the measurement terminal is connectable to a wiring line for connecting any two of the circuit blocks, which is
10 formed in any layer of the semiconductor device;

planar-arranging the measurement terminals and the circuit blocks; and establishing connection of each wiring line, which extends from one of the circuit blocks, via one of the measurement terminals.

The present invention also provides a multilayer semiconductor device which
15 includes a plurality of circuit blocks formed on a semiconductor substrate, the semiconductor device comprises:

measurement terminals, each provided on a wiring line which extends from one of the circuit blocks, wherein each measurement terminal has an electrode formed in an uppermost layer of the semiconductor device and a pad provided in each of the
20 remaining layers of the semiconductor device, and the electrode and the pads are connected with each other via contact holes.

Typically, the positions of the electrode and the pads are substantially the same in plan view.

According to the design method of the present invention, it is possible to very
25 efficiently design a semiconductor device having measurement terminals for performing

electrical measurement which is performed for analyzing the semiconductor device.

The measurement terminals can be automatically arranged using an automatic arrangement tool; thus, the measurement terminals can function as a device for verification performed during design and trial manufacture of the semiconductor device or a measurement and analysis device for quickly analyzing a problem which may appear when the semiconductor device is arranged in a functional system. Therefore, it is possible to considerably reduce the design time. In addition, it is possible to directly observe a portion having a problem, which is actually found by verification, so that a concrete measure for solving the problem can be determined and time necessary for determining such a concrete measure can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing an example of the layout of a semiconductor device, which is designed according to the design method of the present invention.

Fig. 2 is a flowchart for explaining the design method according to the present invention.

Fig. 3 is a diagram showing an example of the cell which is registered in the net list in the circuit arrangement design process.

Fig. 4A is a plan view showing a structure in which some of the circuit blocks and the measurement terminals in Fig. 1 are planar-arranged according to the design method of the present invention. Fig. 4B is a sectional view along line H-H in Fig. 4A.

Fig. 5A is a plan view showing a state in which the circuit blocks and the measurement terminals in Fig. 4 are connected according to the design method of the present invention. Fig. 5B is a sectional view along line H-H in Fig. 5A.

Fig. 6 is a diagram showing an example of the layout for a semiconductor

device, which is designed using a known automatic wiring tool.

Fig. 7A is a diagram showing the wiring structure of area A1 in Fig. 6, and Fig. 7B is a sectional view along line J-J in Fig. 7A.

Fig. 8A is a diagram showing the wiring structure of area A2 in Fig. 6, and Fig. 5 8B is a sectional view along line K-K in Fig. 8A.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments according to the present invention will be explained with reference to the drawings; however, the present invention is not limited to these 10 embodiments.

Fig. 1 is a diagram showing an example of the layout of a semiconductor device, which is designed according to the design method of the present invention. The semiconductor device shown in Fig. 1 has circuit blocks 10A to 10D provided at four corners in the figure, wiring lines extending from each circuit block, and measurement 15 terminals provided on the wiring lines (some of the measurement terminals are indicated by reference numerals 121 to 126). Each of the measurement terminals has a measurement electrode which a probe can contact or which can be irradiated with an electron beam, so as to perform electrical measurement on the uppermost layer of the semiconductor device.

20 In Fig. 1, the circuit block 10A is electrically connected to the circuit block 10B via the wiring lines 134 to 136. More specifically, the terminal 10A6 of the circuit block 10A is connected to the terminal 10B1 of the circuit block 10B via the wiring line 136, and this wiring line 136 electrically connects the circuit blocks 10A and 10B via the measurement terminal 126. The wiring line 134 also electrically connects the circuit 25 blocks 10A and 10B via the measurement terminal 124, and the wiring line 135 also

electrically connects the circuit blocks 10A and 10B via the measurement terminal 125. The terminals 10A1 to 10A3 of the circuit block 10A are connected to the circuit block 10D via wiring lines on which the measurement terminals 121, 122, and 123 are respectively provided.

5 In the semiconductor device of Fig. 1, the wiring lines extending from the circuit blocks 10A to 10D are connected via the measurement terminals; thus, it is possible to very easily perform measurement of the voltage or logic state of each wiring line.

When a problem of any wiring line is found by the measurement, the relevant 10 wiring path is traced and detailed inspection can be performed before or after the relevant circuit block; thus, a defective portion can be directly and easily checked, thereby performing high-speed analysis and reducing the design period of the semiconductor device.

The semiconductor device having the structure as shown in Fig. 1 may be 15 designed by the design method explained below. Fig. 2 is a flowchart for explaining the design method according to the present invention.

As is generally known, in the design of the semiconductor device, a partial circuit having a specific function is designed in each block, and then a chart for connecting inputs and outputs of each circuit (called a "net list") is produced, and a 20 design diagram for manufacturing (i.e., a layout diagram) is produced based on the net list. In the manufacturing of the semiconductor devices, a photomask is produced according to the produced layout diagram, and each layer (for providing transistors, wiring lines, insulating films, or the like) of the semiconductor device is printed on a silicon wafer.

25 The basic procedure of the design method of the present embodiment is similar

to that of the above-explained known design method. That is, as shown in Fig. 2, design of partial circuits (such as circuit blocks and the like) is performed (see step S1), and then circuit arrangement design for producing planar arrangement of the circuit blocks is performed (see step S2). After step S2, circuit connection design for 5 connecting the circuit blocks via wiring lines is performed (see step S3), thereby producing a layout diagram of a semiconductor device (see, for example, Fig. 1). After that, the produced layout diagram is verified (see step S4), and then a mask data is produced (see step S5).

The design method of the present embodiment also has a distinctive step (see 10 step S6) which is not included in the convention method, that is, in step S2 of the circuit arrangement design, the measurement terminals are registered as cells similar to the circuit blocks, so as to perform the automatic layout operation (see step S6). In order to register the measurement terminals as cells, a cell having a structure shown in Fig. 3 may be employed. In Fig. 3, the measurement terminal cell 12 has the main body 12y 15 of the measurement terminal and connecting terminals 13a and 13b (as terminations of the cell) which are connected to the main body 12y via wiring lines. Each of the connecting terminals 13a and 13b is provided for designating connection between wiring lines in the design using an automatic wiring tool or the like, and thus these connecting terminals are not present in the actual semiconductor device. Additionally, Fig. 3 20 shows an example in which two wiring lines extend from the main body 12y of the measurement terminal; however, one, or three or more wiring lines may be connected to the main body 12y of the measurement terminal.

As the circuit blocks used in the automatic layout, each of the circuits, of any 25 scale, from small-scale NAND, OR circuits, and the like, to large-scale operational circuits, memories, and the like, can be registered as a single circuit block (i.e., a cell),

and each wiring line between the blocks is arranged in a manner such that a measurement terminal is provided on the wiring line.

More specifically, in step S2 of the circuit arrangement design in Fig. 2, the measurement terminal cell 12 is arranged, for example, between the circuit blocks 10A and 10B, and in the following step S3 of the circuit connection design, as shown in Fig. 5, the wiring line extended from the terminal 10A-x of the circuit block 10A is connected to the main body 12y of the measurement terminal via the connecting terminal 13a, and the wiring line extended from the terminal 10B-z of the circuit block 10B is connected to the main body 12y of the measurement terminal via the connecting terminal 13b. That is, in the net list used for connecting the wiring lines in the circuit connection design step of the present embodiment, each line of the list includes a measurement terminal between the terminals of the circuit blocks to be connected with each other, for example, "output x of circuit A - measurement terminal y - input z of circuit B" (this example corresponds to the diagram of Fig. 3).

15 Also in the design method of the present embodiment, in step S3 of the circuit connection design, coordinate data of the measurement terminals can also be stored (see step S7). When the coordinate data of the measurement terminals are stored, data of wiring connection between the circuit blocks based on the net list and the position data of each measurement terminal between the circuit blocks can be used in the inspection of 20 the semiconductor device. In addition, the stored coordinate data can also be used in an automatic verification device for verifying the semiconductor device based on the measurement path and the position of each measurement terminal.

A specific example of the process for verifying an output of the circuit block will be explained with reference to Fig. 1. In order to verify an output from the 25 terminal 10A6 of the circuit block 10A, measurement is performed using the

measurement terminal 126 based on the wiring connection data obtained by the net list. so that data (i.e., a logic value) according to an estimated operation (which is estimated in the logic design) is compared with data (i.e., an actual value) indicating the actually-measured logic state. In this process, if the compared data do not coincide 5 with each other, it is estimated that the circuit block A has a problem, or the circuit block 10D positioned before the circuit block 10A has a problem. Therefore, in the next step. measurement is performed using the measurement terminal 121 provided on the input path from the circuit block 10D to the circuit block 10A, and comparison with the logic 10 value is also performed. If the actually measured value and the logic value coincide with each other, it is determined that the circuit block 10A has a problem. and if the actually measured value and the logic value do not coincide with each other, it is determined that the circuit block 10D or a previous circuit block has a problem. Accordingly, the portion having a problem can be very precisely determined by performing measurements along each wiring path between the circuit blocks.

15 Therefore, when the semiconductor device is analyzed, each measurement terminal to be used in the inspection or measurement can be easily known by referring to the net list, and the position data of the measurement terminal can also be easily obtained. Therefore, high-speed and efficient analysis can be performed.

In the above-explained design method for semiconductor devices, almost all 20 steps can be automatically performed by making a computer execute a semiconductor device design program having the following steps. That is, the design program should include a step of arranging the measurement terminals which are registered in the design rules (i.e., the net list) as cells, together with the circuit blocks and the like, and a step of producing wiring between the circuit blocks and the measurement terminals, which are 25 planar-arranged.

The above-explained design method will be explained in more detail, with reference to Figs. 4A to 5B, by referring to an actual structure of the semiconductor device. Fig. 4A is a plan view showing the structure in which the circuit blocks 10A and 10B and the measurement terminals 124 to 126 in Fig. 1 are planar-arranged according to the above-explained design method. Fig. 4B is a sectional view along line H-H in Fig. 4A. Figs. 5A and 5B are a plan view and a sectional view, respectively corresponding to Figs. 4A and 4B, showing the structure after the wiring connection which is performed after the circuit arrangement design shown in Figs. 4A and 4B.

As shown in Fig. 4A, in the step of the circuit arrangement design of the design method in the present embodiment, the measurement terminals 124 to 126 are provided between the terminals 10A4 to 10A6 of the circuit block 10A and the terminals 10B3 to 10B1 (which are respectively connected to the terminals 10A4 to 10A6) of the circuit block 10B, according to the above-explained net list. The measurement terminals 124 to 126 have a similar structure, and the structure of the measurement terminal 126 will be representatively explained. As shown in Fig. 4B, the measurement terminal 126 has a measurement electrode 126a in the uppermost layer of the multilayer semiconductor device, and pads 126b provided in each layer between the first to fifth inter-layer insulating films 21 to 25. The measurement electrode 126a and the pads 126b are provided at the substantially same position in plan view. The adjacent pads are electrically connected via a contact hole 126c which is formed through the inter-layer insulating film between the pads. In addition, the terminal 10A6 of the circuit block 10A is formed between the fifth inter-layer insulating film 25 and the fourth inter-layer insulating film 24, and the terminal 10B1 of the circuit block 10B is formed between the fourth inter-layer insulating film 24 and the third inter-layer insulating film 23.

According to the step S3 of the circuit connection design for performing wiring

between the circuit blocks and the measurement terminals, the wiring lines 134 to 136 for connecting the circuit blocks 10A and 10B via the measurement terminals 124 to 126 are formed, as shown in Figs. 5A and 5B. As shown in Fig. 5B, the measurement terminal 126 has the pad 126b in each layer of the semiconductor device; thus, the 5 terminals 10A6 and 10B1, which are formed in different layers, can be electrically connected by simply forming a wiring line which passes the measurement terminal 126. Therefore, whichever layer (of the semiconductor device) the wiring line for connecting the circuit blocks is formed, electrical measurement can be performed via an electrode formed on the surface of the measurement terminal.

10 In addition, the measurement terminal has a structure in which the contacts (i.e., the contact holes) are stacked (see Fig. 4B). In this case, even when the measurement terminal is provided in the middle of the wiring line, the influence of increase in wiring capacity or variation of impedance can be small.

As explained above, the present embodiment employs the measurement 15 terminals which have a structure as shown in Figs. 4A to 5B; thus, the measurement electrode (see 126a) can be provided on the uppermost layer of the semiconductor device, and wiring connection can be performed in any layer of the semiconductor device, and in addition, the occupied area of the measurement terminal in each layer can be minimized. The measurement electrode should occupy a small area to which a 20 measurement probe can contact; thus, the width of the measurement electrode can be reduced to the width of the wiring line. Therefore, even when high-density wiring having the wiring density as high as that of the conventional wiring is performed, integration degree of the semiconductor device is not influenced. Accordingly, there are fewer limitations on the layout and the design method of the present embodiment can 25 be automated, so that a large number of measurement terminals can be provided at once.

Also in the present design method, each measurement terminal is handled as a cell to be automatically arranged. Therefore, the position of each measurement terminal in plan view can be secured in the automatic arrangement process before the wiring between the circuits is performed. Accordingly, in comparison with the 5 conventional method in which an area for providing each measurement terminal is searched for after the wiring process, the semiconductor device having measurement terminals can be very efficiently designed.

Additionally, in the conventional method in which each hole for measurement is formed in an area on which no wiring line passes, it is necessary that no wiring line 10 pass above a target portion of each wiring line to be measured. In this case, in order to find an area which satisfies the above condition, complicated manual operation should be performed, and if no area which satisfies the condition is found, the entire wiring layout must be reconsidered. However, in the design method according to the present invention, measurement terminals are arranged before the wiring process; thus, the 15 measurement electrode for each measurement terminal is always exposed on the surface of the semiconductor device, so that no manual operation (for searching a target area) as explained above is necessary.

Furthermore, in the present method, the measurement terminal can be provided on each wiring line for connecting the circuit blocks, or the like. Therefore, electrical 20 measurement for verifying or analyzing the semiconductor device can be performed by tracing the wiring lines between the circuit blocks in turn. Accordingly, a portion having a problem can be accurately and quickly determined. In addition, the coordinate data of each measurement terminal can be stored as explained above; thus, it 25 is possible to efficiently perform determination of the position of a measurement probe on the measurement terminal, or the like.

Therefore, when the design method of the present invention is applied to recent semiconductor devices in which an enormous number of circuits are integrated by fine-pattern processing, and thus it is very difficult to determine which portion has a problem, the analysis of the semiconductor device can be accurately performed, and the 5 time necessary for the analysis can be considerably reduced, thereby reducing the design time.